	Alpha 21264	AMD Athlon	Intel PIII	MIPS R12000
Clock rate	700MHz	1000 MHz	1000 MHz	300 MHz
Cache (I/D)	64K/64K	64K/64K	16/16/256	32K/32K
Issue rate	4 issue	3 x 86 instr	3 x 86 instr	4 issue
Pipe stages ‡	7/9 stages	9/11 stages	12/14	6 stages
Out of order	80 Instr	72 ROPs	40 ROPs	48 instr
Rename regs	48/41	36/36	40 total	32/32
BHT entries	4K x 9-bit	4K x 2-bit	≥512	2K x 2-bit
TLB entries	128/128	280/288	32 1/64 D	64 unified
Memory B/W	2.66 GB/s	1.6 GB/s	1.06 GB/s	539 MB/s
Package	CPGA-588	CBGA-576	PGA-370	CPGA-527
IC process	0.25µ 6M	0.18µ 6M	0.18µ 6M	0.25µ 4M
Die size	205 mm^2	102 mm^2	106 mm^2	204 mm^2
Transistors	15.2 million	22 million	24 million	7.2 million
Est mfg cost*	$160	$70§	$40	$140
Power (max)	75 W	60 W*	23 W*	20 W
SPEC95b†	35/55	42/30	47/32	18/30
Availability	3Q99	1Q00	1Q00	2Q99
1K list price	$2,296§§	$1299§	$990	Not public

A

B

C

†SPEC95 baseline (int/FP) ‡integer ALU/load §indudes 512K L2 cache

CONVENTIONAL ART

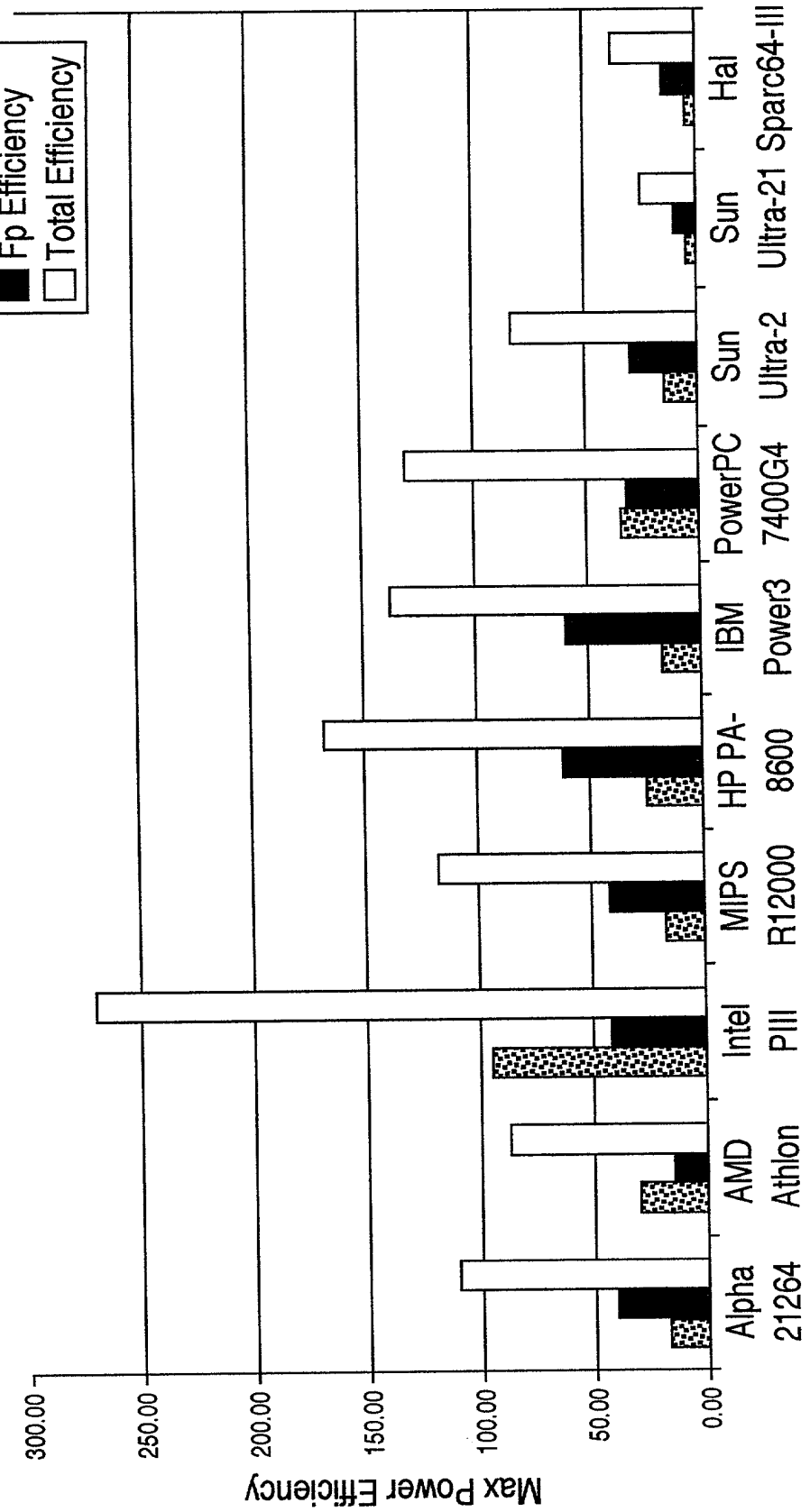
Fig. 1

HP PA-8600	IBM Power3	PowerPC 7400 (G4)	Sun Ultra-2	Sun Ultra-21	Hal Sparc64-III
552 MHz	400 MHz	450 MHz	450 MHz	360 MHz	296 MHz
512K/1M	32K/64K	32K/32K	16K/16K	16K/16K	64K/64K
4 issue	4 issue	3 issue	4 issue	4 issue	4 issue
7/9 stages	7/8 stages	4/5 stages	6/9 stages	6/9 stages	8/10
56 instr	32 instr	5 instr	None	None	63 instr
56 total	16 int/24 fp	6 int/6 fp	None	None	34/32
2K x 2-bit	2K x 2-bit	512 x 2-bit	512 x 2-bit	512 x 2-bit	8K x 2-bit
120 unified	128/128	128/128	641/64D	641/64 D	32/32/256
1.54 GB/s	1.6 GB/s	1.6 GB/s	1.9 GB/s	600 MB/s	1.33 GB/s
LGA-544	SCC-1,088	CBGA-360	CLGA-787	PBGA-587	CLGA-957
0.25µ 4M	0.22µ 6M	0.22µ 6M	0.29µ 4M	0.29µ 4M	0.25µ 5M
477 mm^2	163 mm^2	83 mm^2	126 mm^2	150 mm^2	240 mm^2
130 million	23 million	10.5 million	3.8 million	4.1 million	17.6 million
$330	$110	$45	$70	$85	$250
60 W*	36 W	13 W	20 W	38 W	50 W
39/61	24/46	21/20	16/24	12/17	15/28
1Q00	1Q00	3Q99	4Q98	4Q98	4Q98
Not public	Not public	$345	$4,249§§	$470	Not public

§§indudes 2M L2 cache (Source: vendors, except *MDR estimates)

CONVENTIONAL ART

Fig. 1 Continued



CONVENTIONAL ART

Fig. 2

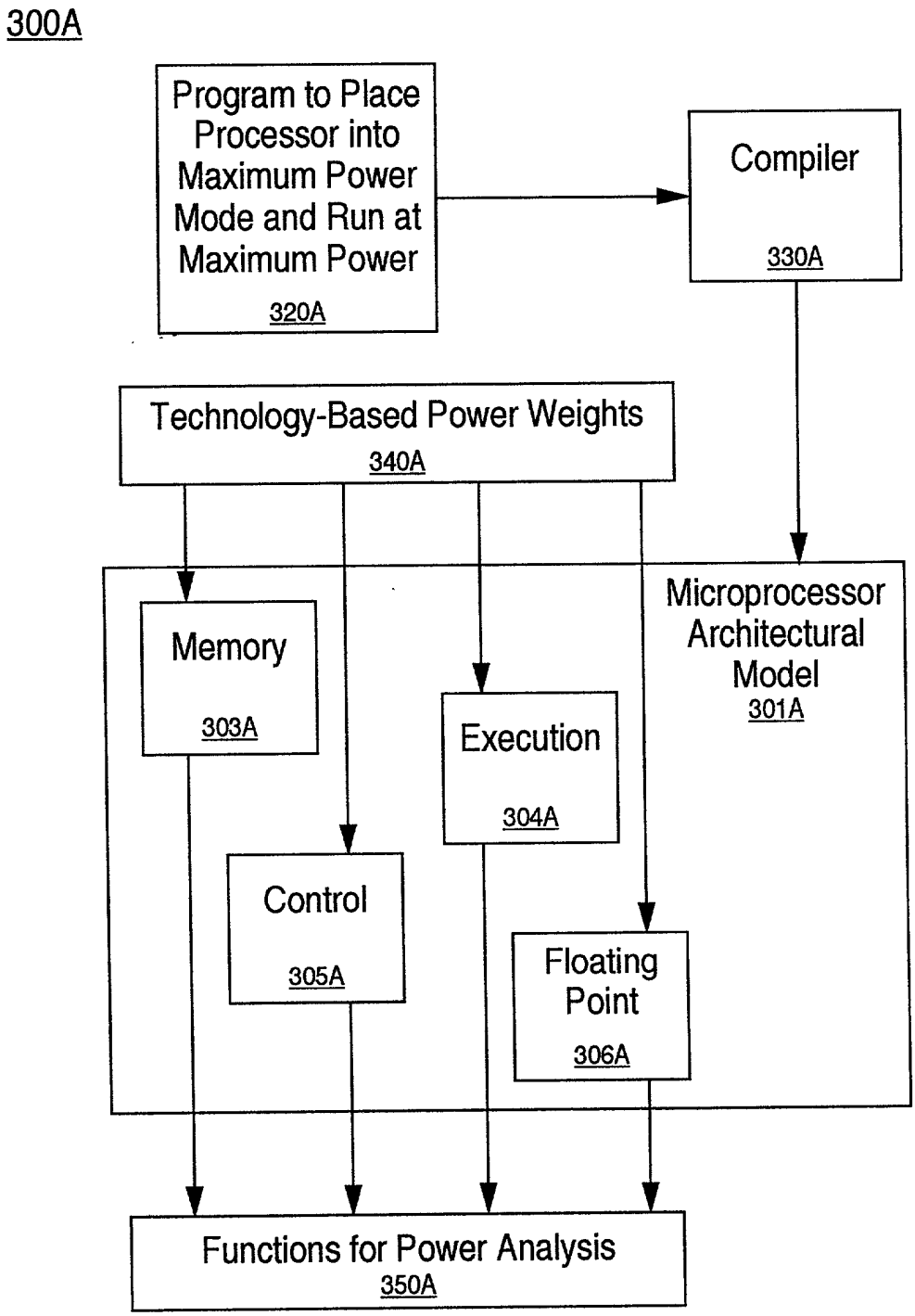

300A
Program to Place Processor into Maximum Power Mode and Run at Maximum Power
320A
Compiler
330A
Technology-Based Power Weights
340A
Memory
303A
Execution
304A
Microprocessor Architectural Model
301A
Control
305A
Floating Point
306A
Functions for Power Analysis
350A

Fig. 3A

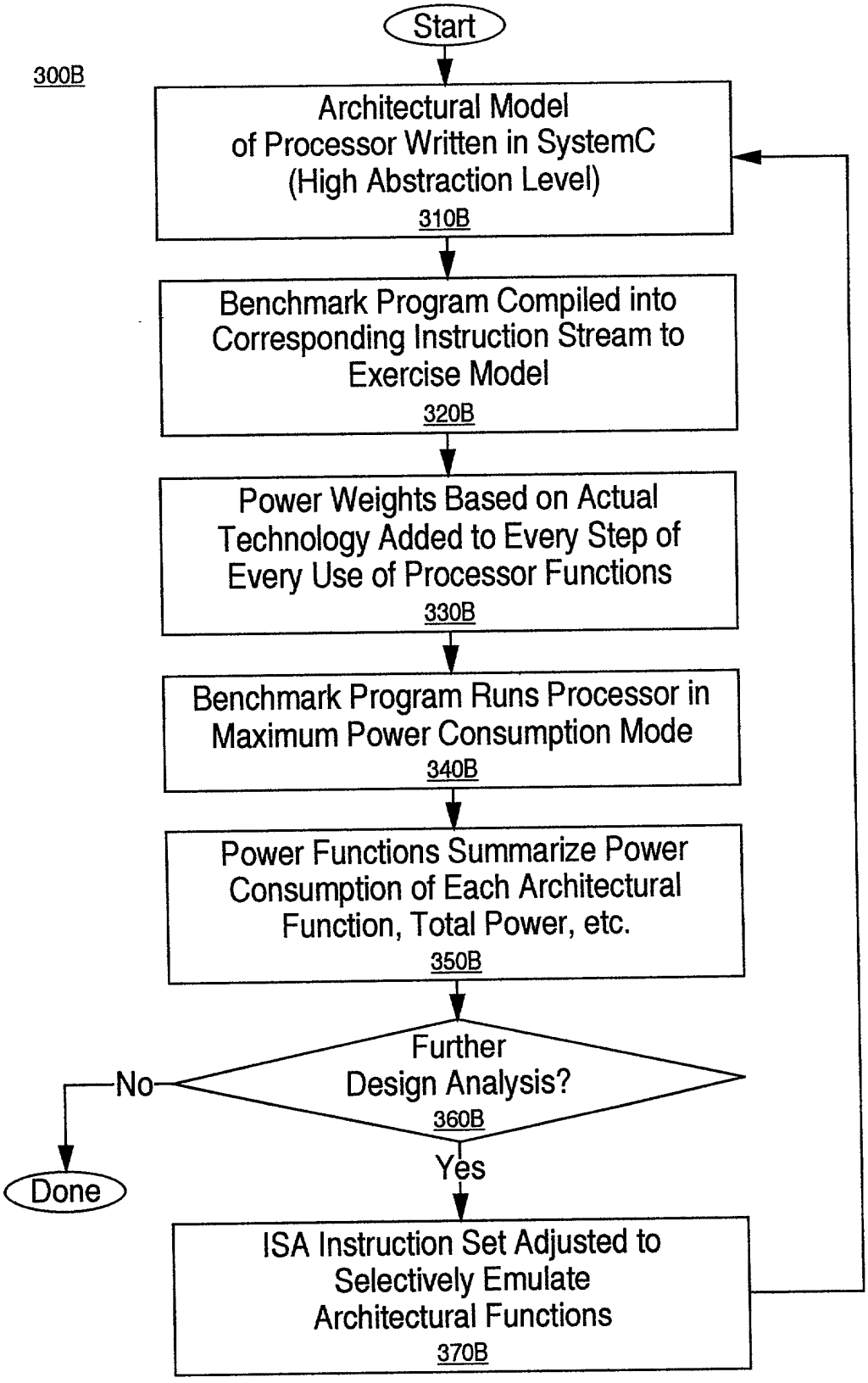

300B
Start
Architectural Model of Processor Written in SystemC (High Abstraction Level)
310B
Benchmark Program Compiled into Corresponding Instruction Stream to Exercise Model
320B
Power Weights Based on Actual Technology Added to Every Step of Every Use of Processor Functions
330B
Benchmark Program Runs Processor in Maximum Power Consumption Mode
340B
Power Functions Summarize Power Consumption of Each Architectural Function, Total Power, etc.
350B
Further Design Analysis?
360B
No
Yes
Done
ISA Instruction Set Adjusted to Selectively Emulate Architectural Functions
370B

Fig. 3B

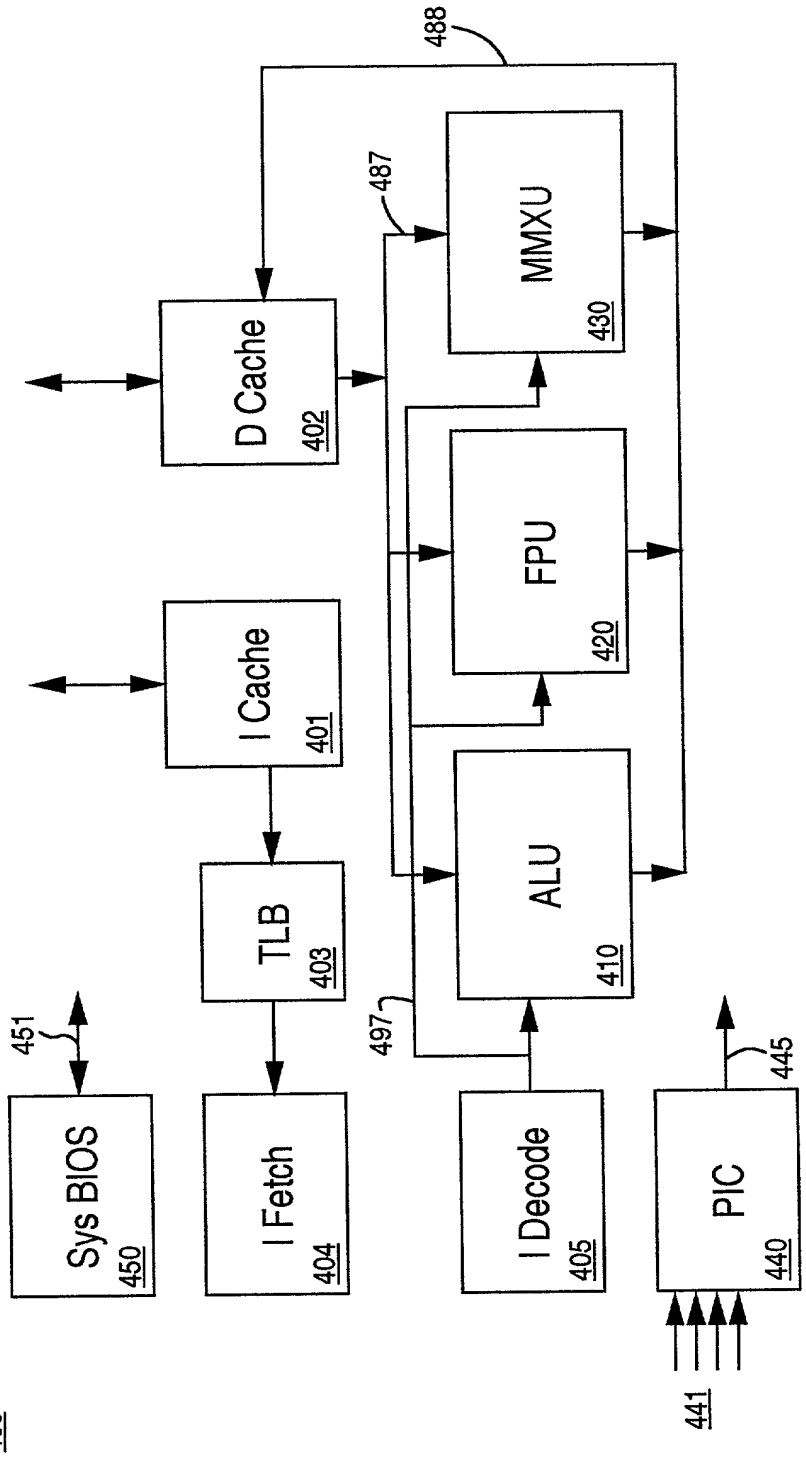

400
Sys BIOS
450
451
I Fetch
404
TLB
403
I Cache
401
D Cache
402
I Decode
405
ALU
410
497
FPU
420
MMXU
430
487
488
PIC
440
445
441

Fig. 4A

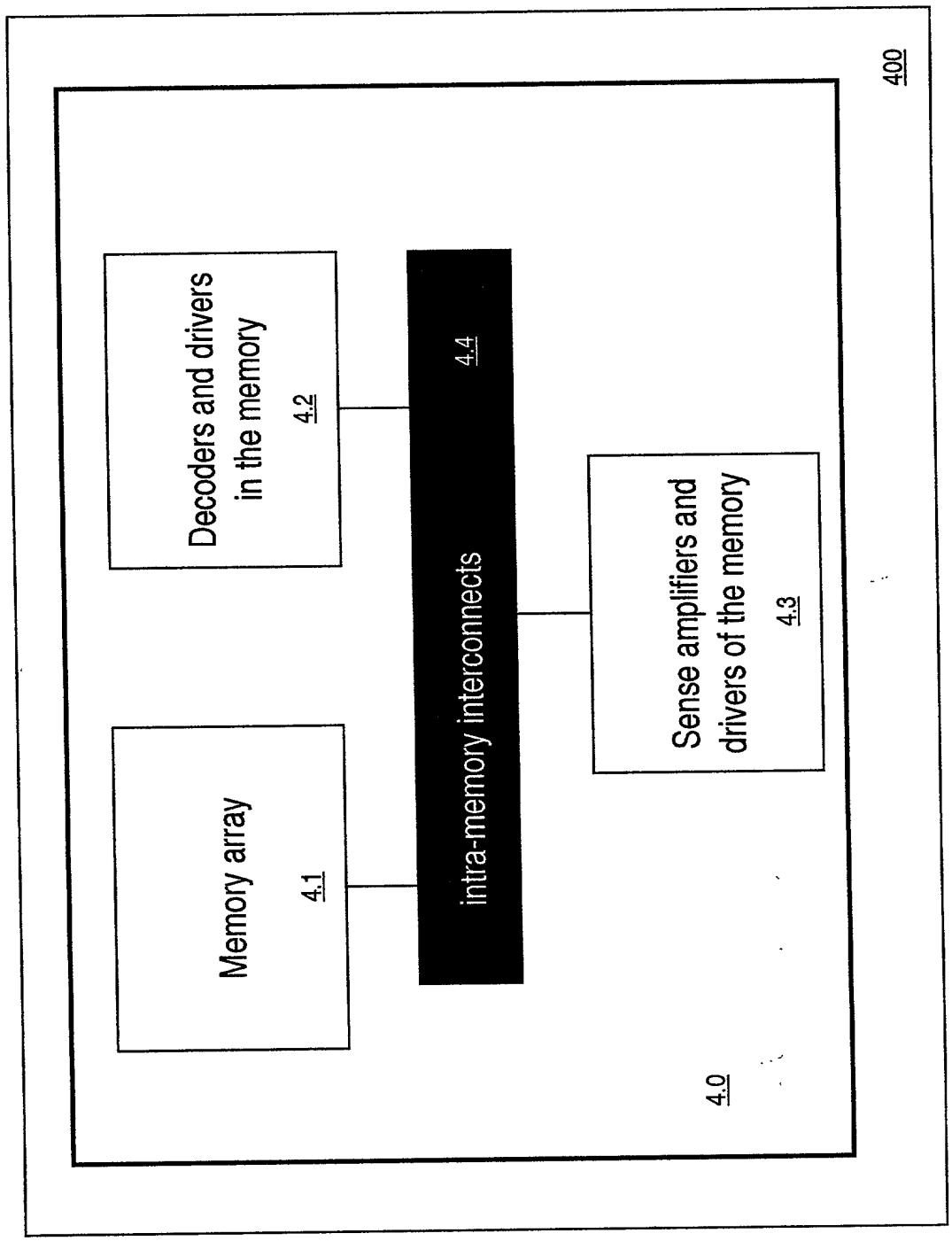

400
4.0
Memory array
4.1
Decoders and drivers in the memory
4.2
intra-memory interconnects
4.4
Sense amplifiers and drivers of the memory
4.3

Fig. 4B

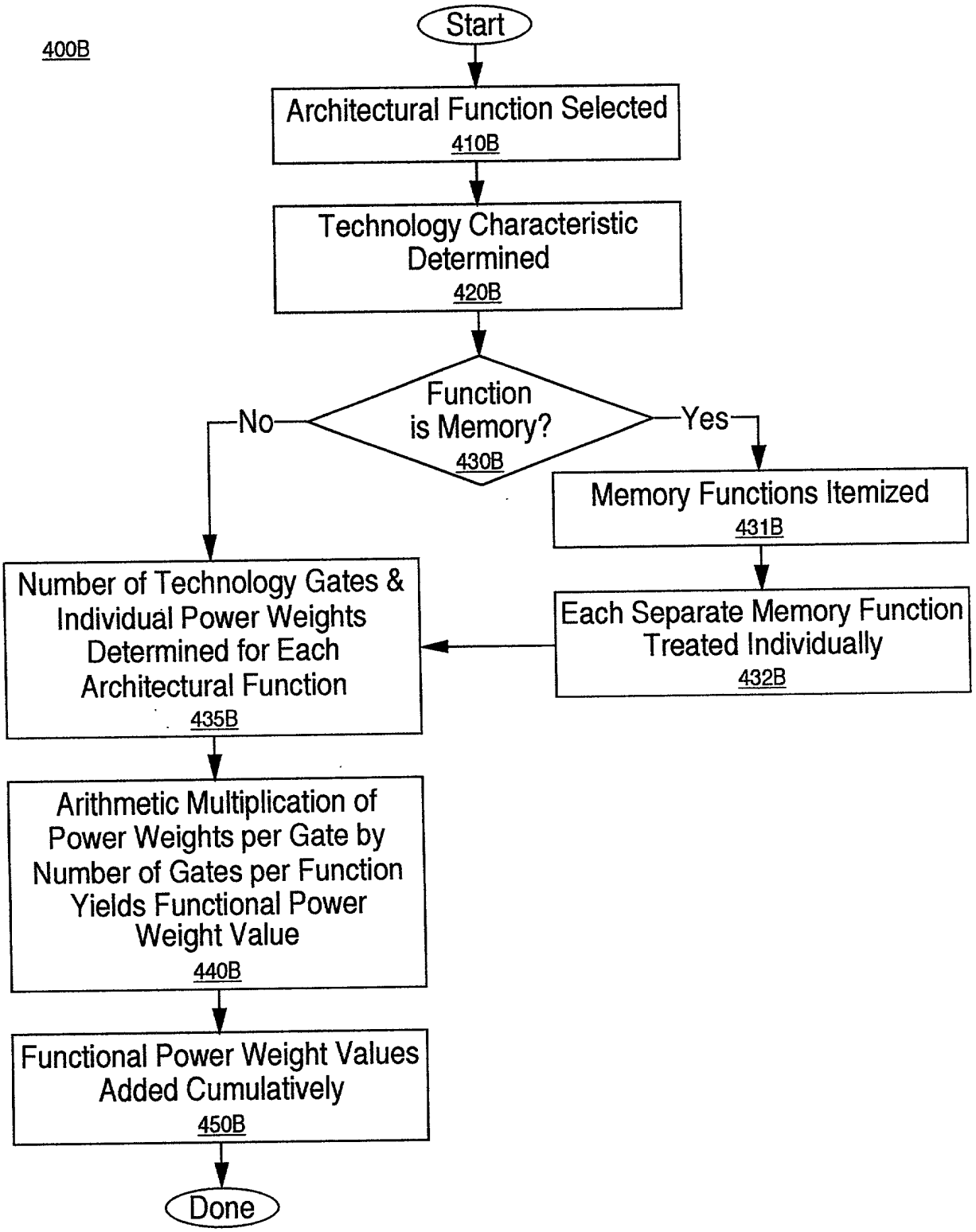

400B
Start
Architectural Function Selected
410B
Technology Characteristic Determined
420B
Function is Memory?
430B
No
Yes
Memory Functions Itemized
431B
Each Separate Memory Function Treated Individually
432B
Number of Technology Gates & Individual Power Weights Determined for Each Architectural Function
435B
Arithmetic Multiplication of Power Weights per Gate by Number of Gates per Function Yields Functional Power Weight Value
440B
Functional Power Weight Values Added Cumulatively
450B
Done

Fig. 4C

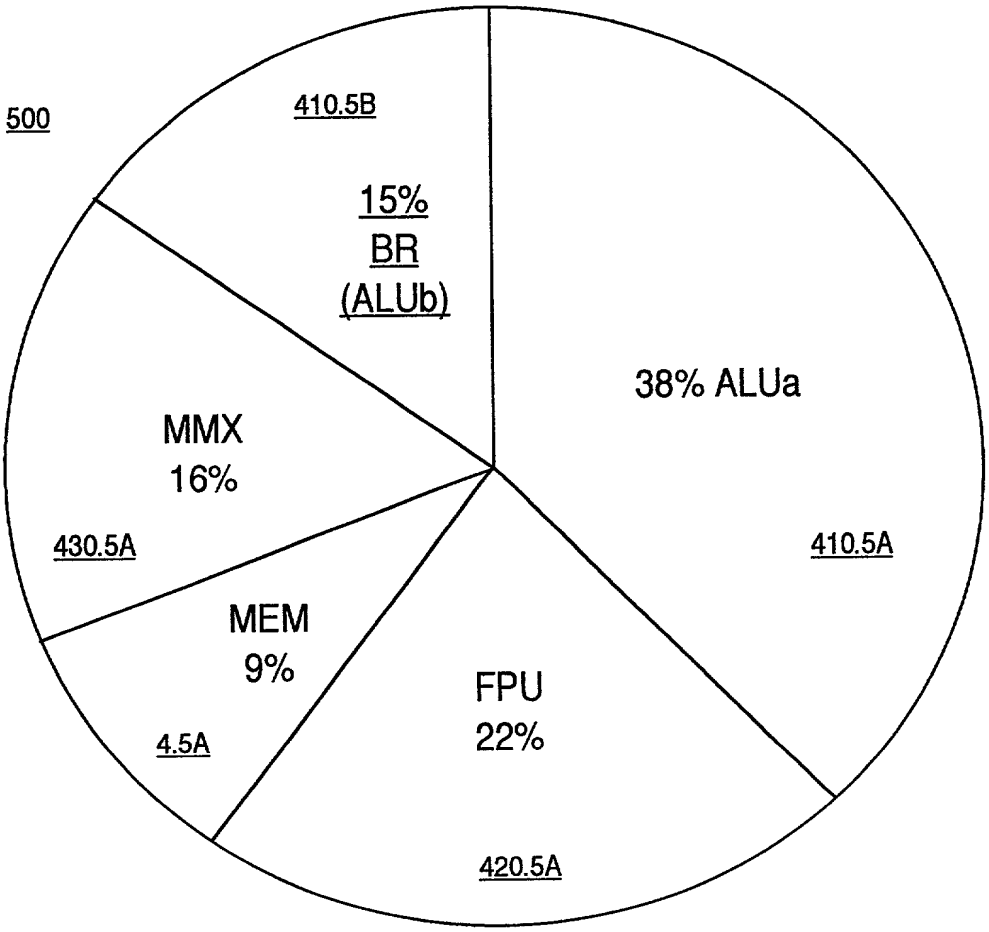


Fig. 5A

Docket No. 2003P13121US

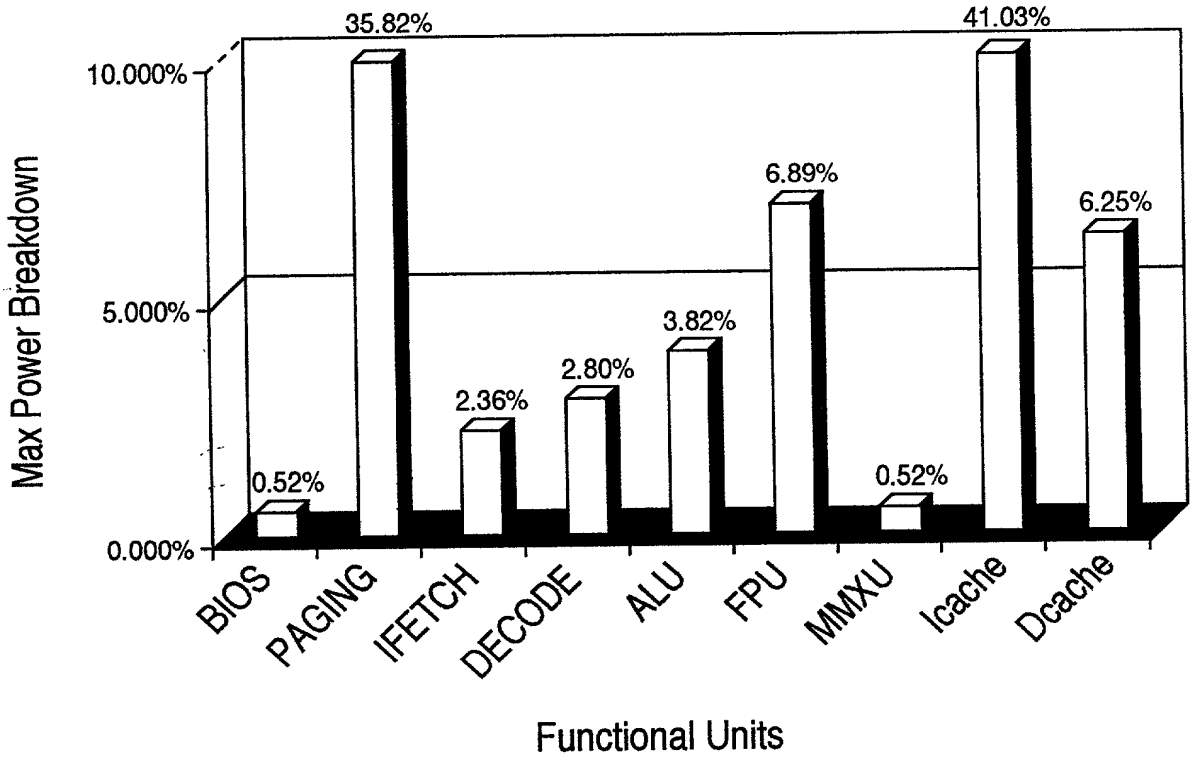

Max Power Breakdown
10.000%
5.000%
0.000%
35.82%
41.03%
6.89%
6.25%
3.82%
2.80%
2.36%
0.52%
0.52%
BIOS
PAGING
IFETCH
DECODE
ALU
FPU
MMXU
Icache
Dcache
Functional Units

Fig. 5B

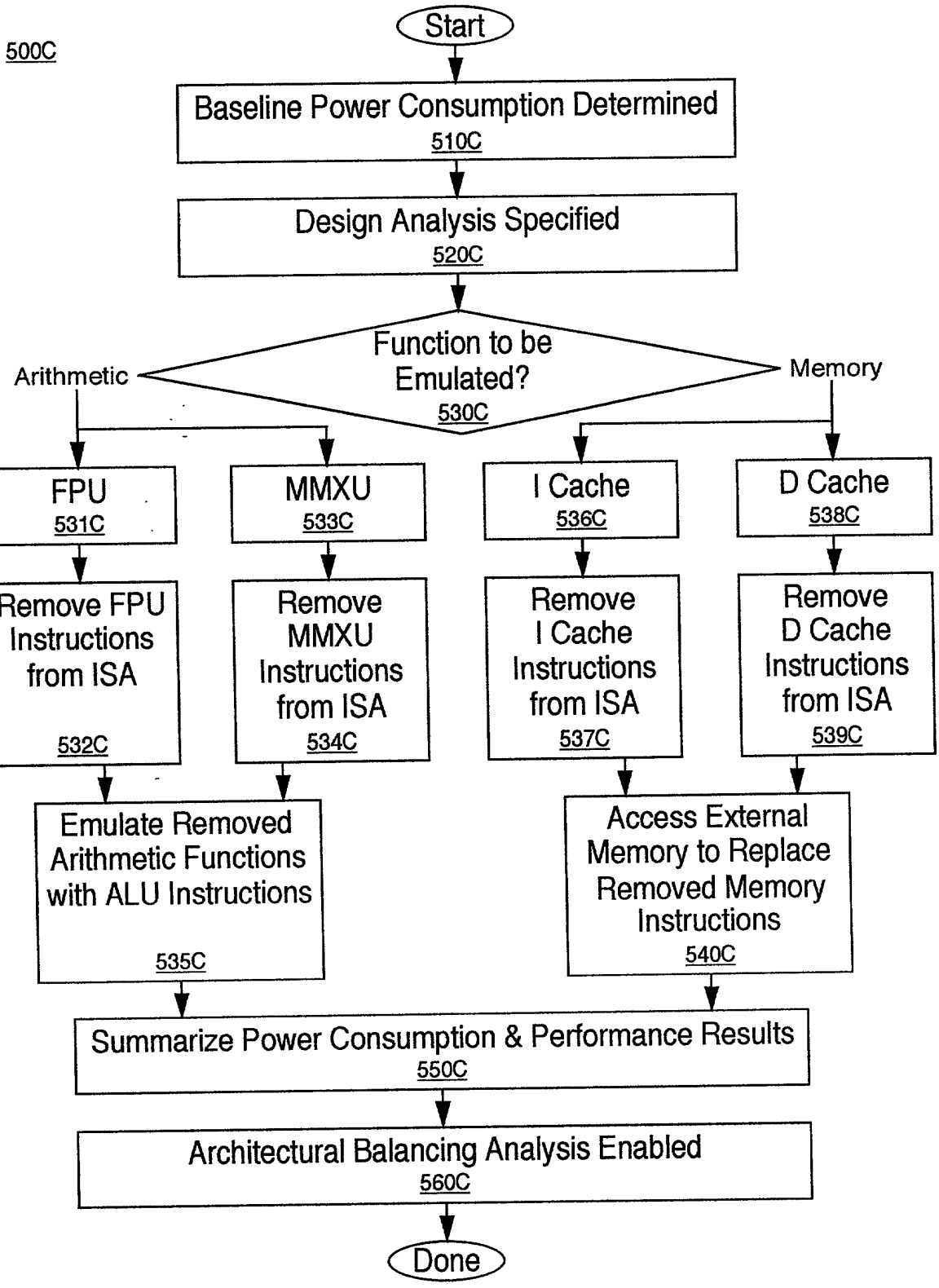


Fig. 5C

Docket: 042390.P12104